

Adeel Akhtar

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Summary

Senior FPGA and Embedded Systems Engineer with 10+ years of industrial experience in FPGA architecture, hardware/software co-design, camera ISP, cybersecurity, high-frequency trading, hyperspectral imaging, ADAS, and autonomous driving. Strong expertise in VHDL, C/C++, HLS, UVM, MATLAB, and Python, with extensive experience in FPGA design, verification, integration, and hardware debugging across a wide range of embedded systems. Proven experience in developing high-performance, reusable, and production-ready FPGA solutions, as well as providing technical leadership and mentoring engineering teams.

Technical Expertise

HDL & Programming: VHDL, HLS, C/C++, Python, MATLAB, Tcl.

FPGA/RTL: FPGA Architecture, Pipelining, CDC, Timing Closure, Synthesis, Resource and Latency Optimization.

Verification: VUnit, OSVVM, UVM, RTL Simulation, ILA/VIO, Hardware Debugging.

Tools: Vivado, Vitis HLS, Quartus, Libero SoC, QuestaSim, ModelSim, Git, Jenkins.

Platforms: Alveo U250, Zynq-7000, Zynq UltraScale+ MPSoC, ZCU102, Intel/Altera, PolarFire.

Interfaces: AXI/AXI-Stream, PCIe, Ethernet, I²C, I²S, SPDIF, CAN, USB, HDMI, MIPI, FPD-Link III, UART and SPI.

Domains: Low-Latency/HFT, Video/ISP, Analog/Digital Audio Processing, Cybersecurity, ADAS, Autonomous Driving Cameras, Industrial & Hyperspectral Imaging.

Work Experience

11/2024 – Present

IHSE GmbH, Oberteuringen, Germany.

Senior Firmware Engineer (FPGA Systems)

- Architected high-performance solutions for video, imaging and low-latency processing.
- Designed FPGA cybersecurity solutions using AES and GCM encryption.
- Implemented digital and analog audio interfaces including S/PDIF, codecs, and ADC/DAC.
- Created real-time On-Screen Display (OSD) overlays for video systems.
- Defined hierarchical architectures integrating reusable IP and high-speed interfaces.
- Built platform-independent verification using VUnit, Riviera, QuestaSim, and ModelSim.
- Adapted solutions across multiple FPGA vendors and technology platforms.
- Executed hardware bring-up, system integration, debugging, and validation.
- Led development activities, mentoring, timing closure, hardware debugging, and production readiness.

11/2021 – 09/2024

360T/Deutsche Börse Group, Frankfurt am Main, Germany.

Senior Engineer - FPGA Hardware/Software Codesign

- Designed ultra-low latency pipeline solution for high-frequency trading in fintech.
- Multiple data feeds from Foreign Exchange (FX) using FIX and Binary protocols.
- Developed high-performance algorithms tailored to the business model.
- Managed Order Book Memory for real-time price and trade updates.

- Utilized AMD/Xilinx Alveo U250 FPGA with HLS (C/C++) and VHDL.
- Created APIs for efficient traffic management between CPU and FPGA.
- Integrated third-party IPs to enhance product functionality.
- Applied UVM for comprehensive design functional verification.
- Served as Scrum Master, managing tasks via Jira and Git.
- Delivered in-house FPGA training, significantly improving team expertise.

07/2017 – 10/2021

Hyundai Mobis, Frankfurt am Main, Germany.

Senior Embedded Systems Engineer (ADAS and Autonomous Driving)

- Developed an Image Signal Processor (ISP) pipeline for front end cameras.
- Tuned ISP and developed algorithms for camera image quality assessment.
- Implemented algorithms on FPGA platforms (Xilinx: ZCU102, Zynq 7020 and Alveo).
- Utilized interfaces including I2C, UART, SPI, CAN, AXI-Lite, and AXI-Stream.
- Benchmarked technology solutions from Xilinx, NVIDIA, and Texas Instruments (TDA4x).
- Created multithreaded modules using RTMaps for system testing.
- Performed DNN performance analysis and validation on target hardware platforms.
- Provided training on Mobis tools to production units globally.
- Utilized MATLAB for algorithm validation and block verification.
- Managed continuous development tasks as Scrum Master, utilizing Jira and Git.
- Coordinated technically with customers and suppliers on active projects.

12/2015 – 05/2017

Inno-Spec GmbH, Nürnberg, Germany.

Development Engineer Embedded Systems (Industrial Cameras)

- Developed ISP pipeline for high-speed hyperspectral imaging cameras.
- Programmed FPGA modules in VHDL for Xilinx FPGAs (Artix-7 and Kintex-7 series).
- Established sensor communication via AXI, Wishbone, I2C, SPI, and other interconnects.
- Developed soft IPs using high-level synthesis (HLS) for precise hardware implementation.
- Created MATLAB-based testing tools for image enhancement.
- Designed and developed intuitive GUI for seamless user interaction.
- Collaborated with customers and partners to develop strategic solutions.

04/2013 – 03/2015

Control System Research Group, TU Kaiserslautern, Germany.

Research Assistant, (Industrial Projects)

- Developed sensor fusion routines for inertial navigation systems using Kalman Filter
- Created instrument drivers for the Raspberry Pi platform using Python.
- Developed heuristic control algorithms to optimize battery charging efficiency.
- Designed GUI, analysed data, and visualized and simulated algorithms in MATLAB.
- Implemented real-time data communication on ARM Cortex-M4 microcontroller using C.
- Documented the programming framework and conducted simulation studies.

10/2013 – 04/2014

Microelectronic Systems Design Group, TU Kaiserslautern, Germany.

Research Assistant

- Designed FPGA architecture for a soft demapping algorithm in digital wireless receivers.
- Analysed algorithm communication performance using C++ and MATLAB.
- Documented and developed an equivalent bit-true C model.
- Implemented the module in synthesizable VHDL for FPGA deployment.
- Verified the module across all combinations to ensure accuracy and reliability.

06/2010 – 06/2011

Nespak Engineering Company, Pakistan.

Trainee Engineer

- Supervised tasks on field and designed electric circuits.
- Client meetings to ensure quality standards.

09/2008 – 08/2010 **Teaching in Rawalpindi Institute of Technology, Pakistan.**

- Electric Circuits Design.
- Applied Engineering Mathematics.

Education

04/2012 – 09/2015 **Technical University of Kaiserslautern, Germany.**
M.Sc. Electrical and Computer Engineering (Embedded Systems)
Final Grade: 2.2 (German Scale), A- (U.S. Scale)

Master Thesis

Design Space Exploration for Autocorrelation-Based Frequency Offset Estimation in FPGA

- Investigated algorithms for Digital Video Broadcasting (DVB-RCS2) in satellite communication applications.
- Implemented and analysed the communication performance of the proposed algorithms in both the time and frequency domains using C++.
- Developed bit-true C models for time and frequency domain algorithms.
- Conducted hardware implementation of both architectures in VHDL for the smallest Xilinx FPGA devices.
- Verified software and hardware models across all combinations.
- Evaluated the implemented architectures based on implementation complexity, throughput, latency, and hardware resource requirements in FPGA devices.

08/2005 – 01/2010 **Federal Urdu University of Arts, Science and Technology, Pakistan.**
B.Sc. Electrical Engineering (Electronics/Communication)
Final Grade: 1.2 (German Scale), 3.82 (U.S. Scale)

Bachelor Thesis

Channel Estimation and Equalization of OFDM (Orthogonal Freq Division Multiplexing) Systems

Languages

English: Fluent

German: Good

Urdu/Punjabi: Native language

Achievements

- Award winner at the AMD/Xilinx Adaptive Computing Summit, Frankfurt, Germany (2024).
- Awarded Lenovo Explorer mixed reality headset at Nvidia's GTC Munich, Germany (2017).
- Awarded best performance certificate by Muslim Students Group (MSG) Kaiserslautern, Germany (2015).
- Received Best Performance Award as Finance Secretary, Pakistan Student Association (2014).
- Achieved 3rd place in Telenor Audition Karo Mumkin (Islamabad Division, 2010).
- Awarded talent scholarship by MAJU (Mohammad Ali Jinnah University), Pakistan (2010).
- Received the Best Performance Award from the Belgium Institute of Peace and Development at the Leadership Conference and Ceremony (2008).

References

Available on request